INTERSIL
SYSTEMS DIVISION

ICP/M 395
IMAC 245
IFORT 765
IBASI 610
IBASIC COMP 610
PASCAL 775

ISB-3400 Floppy Disk Controller Card

599

FEATURES

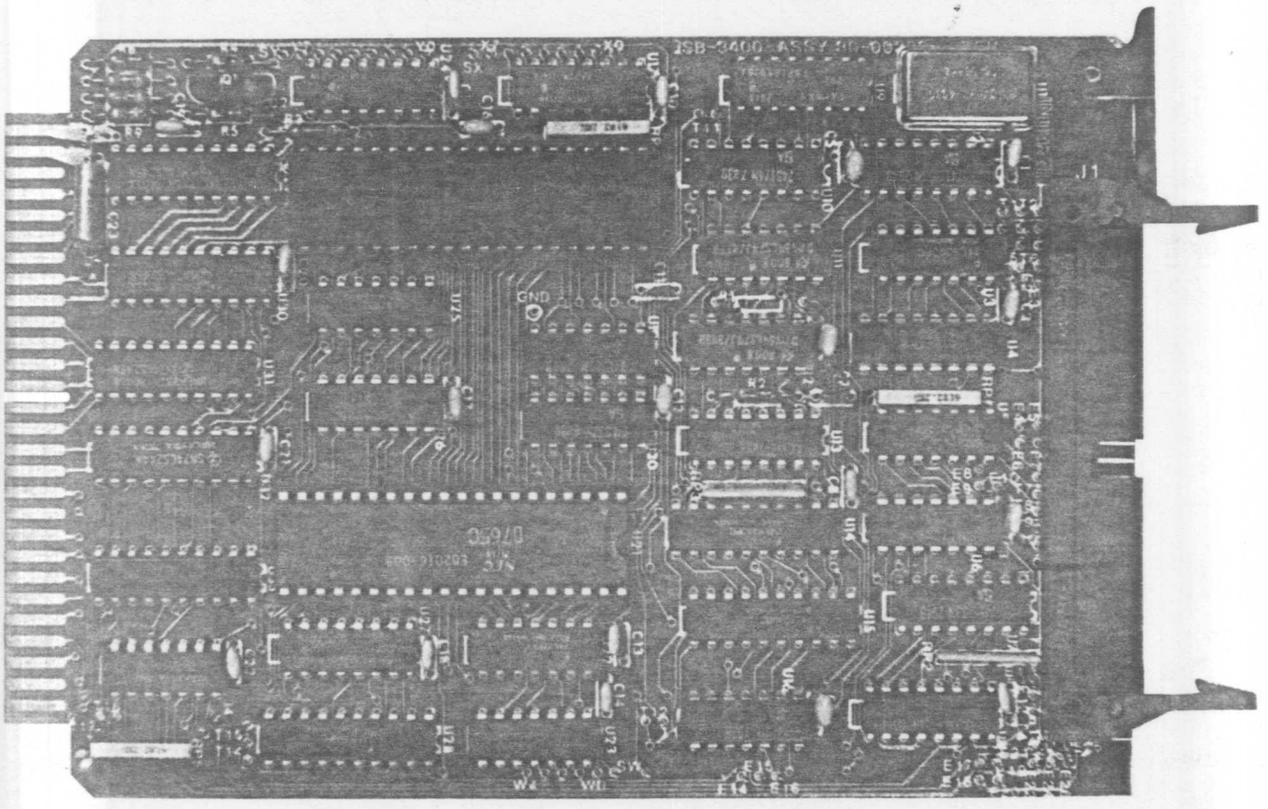
- Full STD BUS Compatibility
- Double (MFM) or Single (FM) Density Operation-Software Selectable
- Double or Single Sided Operation - Software Selectable
- On-Card Direct Memory Access Controller
- Controls Up to Four Floppy Disk Drives - 8 Inch or 5.25 Inch Jumper Selectable
- Compatible with IBM 3740, IBM System 34 and other Soft-Sectored Formats
- Diskett Initialization
- Automatic CRC Generation and Checking
- Single-Sector, Multiple-Sector and Multiple-Track Transfer Capability
- DMA, Interrupt-Driven, or Polled Operation
- Digital Phase Lock Loop Data Recovery Circuit
- Wait States Jumper Selectable
- Requires +5V Only

GENERAL DESCRIPTION

The ISB-3400 is a STD BUS Floppy Disk Controller Card which can control, write to and read from up to four single or double density, single or double sided, drives. The card will operate with Z80 based and 8085 based microprocessor cards, up to a 4 MHz clock frequency. It is totally compatible with the ISB-3100 and the ISB-3110 Processor Cards.

The card contains an LSI Floppy Disk Controller circuit and an LSI Direct Memory Access Controller. An extra output register provides optional drive control lines. Precompensation circuitry provides jumper selectable amounts of write data precompensation. A digital phase lock loop circuit using a sequencer ROM provides reliable read data recovery including the inner tracks of double density diskettes.

Connection to both 8 inch and 5.25 inch floppy disk drives is made via a single fifty-pin ribbon cable connector with ejectors. Jumpers are available to allow operation with a wide variety of disk drive options, including individual motor control for 5.25 inch drives.



INTERSIL, INC., Systems Division, 1275 Hammerwood Avenue, Sunnyvale, CA 94086 (408) 743-4442 TWX: 910-339-9369

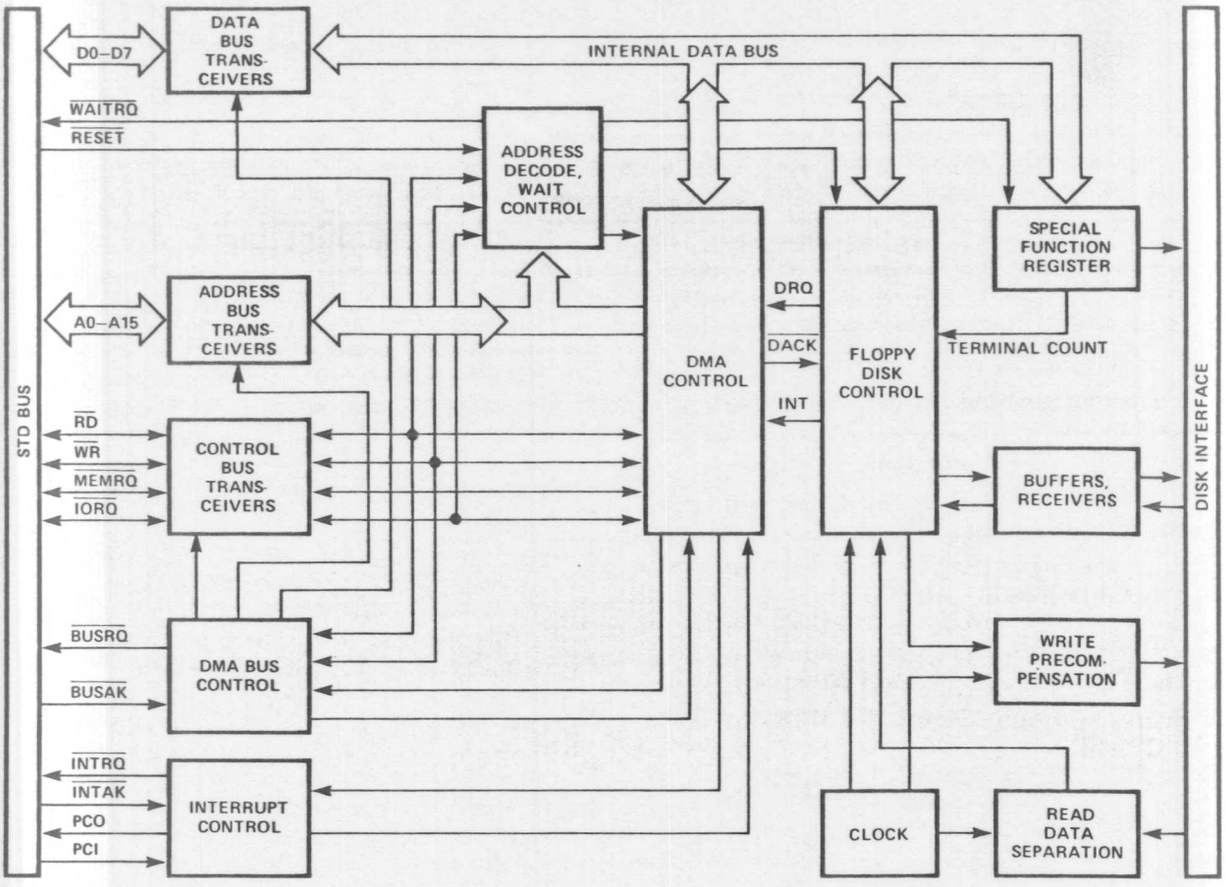


FIGURE 1. ISB-3400 Block Diagram

SPECIFICATIONS

Power Requirements:	+5 VDC at less than 1.0 Amp, 5 watts max.
Address Selection:	Lowest port address selectable within range 00 to FC, in increments of four – selected with jumpers
Interface:	All STD BUS address, data and command signals are TTL compatible. Disk output lines are open collector TTL, disk input lines are TTL compatible with hysteresis
Input Loading:	One TTL low-power Schottky load per input
Mating Connectors:	See Table 1
Card Dimensions:	Height (with ejectors): 7.18 inches (18.24 cm) Width 4.48 inches (11.39 cm) Thickness: 0.40 inches (1.016 cm)
Word Size:	Eight bits
I/O Capacity:	Up to four megabytes of Floppy Disk Storage can be accessed
Direct Memory Access:	A single transfer between disk drive and memory can be from 128 bytes to 16,384 bytes

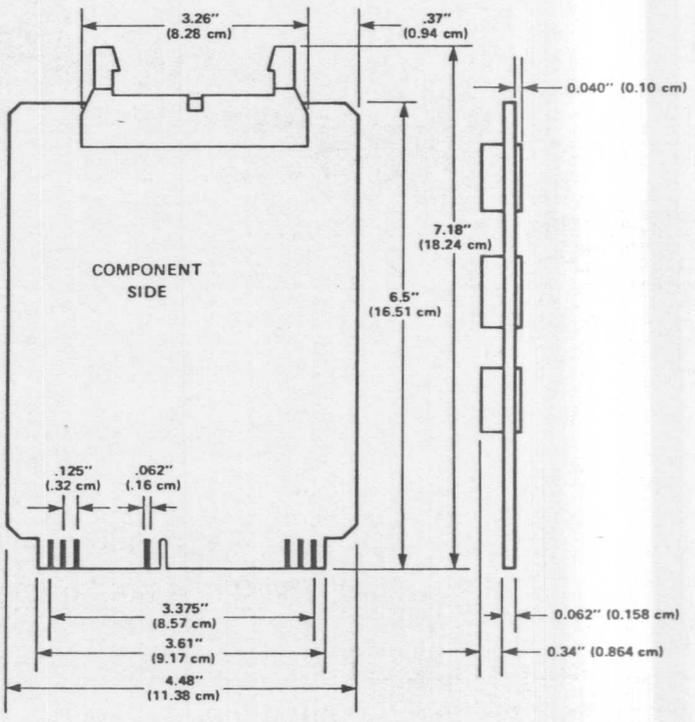


FIGURE 2. ISB-3400 Physical Dimension Diagram

ENVIRONMENTAL REQUIREMENTS

Operating Temperature: 0°C to 55°C
Storage Temperature: −40°C to 80°C
Relative Humidity: 0% to 90% without condensation

TABLE 1. ISB-3400 Compatible Mating Connectors

INTERFACE	NO. OF PINS	CENTERS	CONNECTOR TYPE	VENDOR	VENDOR PART NO.	KEYED
STD BUS	56	0.125 in.	Solder Tail	Viking Winchester	VH28/ICNK5 2HW D0−111	Between Pins 26 and 28
STD BUS	56	0.125 in.	Wire Wrap	Viking Winchester	VH28/ICND5 HW28 D0−111	Between Pins 26 and 28
Disk Drive	50	0.1 in. by 0.1 in.	Insulation Displacement	3M	3425 Series	Optional
				Berg.	65484 Series	

TABLE 2. ISB-3400 STD BUS Organization and Functional Specifications (With Pin Definitions)

The STD BUS pinout is organized into five functional groups:

Logic Power Bus	Pins 1−6
Data Bus	Pins 7−14
Address Bus	Pins 15−30
Control Bus	Pins 31−52
Auxiliary Power Bus	Pins 53−56

COMPONENT SIDE				CIRCUIT SIDE			
PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION
1	+5V	In	+5 Volts DC (Bussed)	2	+5V	In	+5 Volts DC (Bussed)
3	GND	In	Digital Ground (Bussed)	4	GND	In	Digital Ground (Bussed)
5	−5V	In	−5 Volts DC	6	−5V	In	−5 Volts DC
7	D3	In/Out	Low Order Data Bus	8	D7	In/Out	High Order Data Bus
9	D2	In/Out	Low Order Data Bus	10	D6	In/Out	High Order Data Bus
11	D1	In/Out	Low Order Data Bus	12	D5	In/Out	High Order Data Bus
13	D0	In/Out	Low Order Data Bus	14	D4	In/Out	High Order Data Bus
15	A7	Out	Low Order Address Bus	16	A15	Out	High Order Address Bus
17	A6	Out	Low Order Address Bus	18	A14	Out	High Order Address Bus
19	A5	Out	Low Order Address Bus	20	A13	Out	High Order Address Bus
21	A4	Out	Low Order Address Bus	22	A12	Out	High Order Address Bus
23	A3	Out	Low Order Address Bus	24	A11	Out	High Order Address Bus
25	A2	Out	Low Order Address Bus	26	A10	Out	High Order Address Bus
27	A1	Out	Low Order Address Bus	28	A9	Out	High Order Address Bus
29	A0	Out	Low Order Address Bus	30	A8	Out	High Order Address Bus
31	$\overline{WR}$	Out	Write to Memory or I/O	32	$\overline{RD}$	Out	Read to Memory or I/O
33	$\overline{IORQ}$	Out	I/O Address Select	34	$\overline{MEMRQ}$	Out	Memory Address Select
35	$\overline{IOEXP}$	In/Out	I/O Expansion	36	$\overline{MEMEX}$	In/Out	Memory Expansion
37	$\overline{REFRESH}$	Out	Refresh Timing	38	$\overline{MCSYNC}$	Out	CPU Machine Cycle Sync
39	$\overline{STATUS\ 1}$	Out	CPU Status	40	$\overline{STATUS\ 0}$	Out	CPU Status
41	$\overline{BUSAK}$	Out	Bus Acknowledge	42	$\overline{BUSRQ}$	In	Bus Request
43	$\overline{INTAK}$	Out	Interrupt Acknowledge	44	$\overline{INTRQ}$	In	Interrupt Request
45	$\overline{WAITRQ}$	In	Wait Request	46	$\overline{NMIRQ}$	In	Non-Maskable Interrupt
47	$\overline{SYSRESET}$	Out	System Reset	48	$\overline{PBRESET}$	In	Push Button Reset
49	$\overline{CLOCK}$	Out	Clock from Processor	50	$\overline{CNTRL}$	In	AUX Timing
51	PCO	Out	Priority Chain Out	52	PCI	In	Priority Chain In
53	AUX GND	In	AUX Ground (Bussed)	54	AUX GND	In	AUX Ground (Bussed)
55	AUX+V	In	AUX Positive (+12 Volts DC)	56	AUX−V	In	AUX Negative (−12 Volts DC)

TABLE 3. ISB-3400 STD BUS Signal Definitions

SIGNAL	PIN NO.	FUNCTIONAL DESCRIPTION
+5V	1 & 2	*+5 Logic Voltage (V_{CC})* – Main logic voltage lines (+5 volts). Both pins are bussed together for current capacity.
GND	3 & 4	*Logic Ground* – Ground for logic power. Both pins are bussed together for current capacity.
–5V	5 & 6	*–5 Logic Voltage* – Auxiliary Logic Voltage. (Not used on the ISB-3400).
D0–D7	7–14	*Data Bus* – An 8-Bit bidirectional tri-state bus. (Bidirectional means signals may flow either into or out of any card on the Bus). Direction of data is controlled by the processor card via the Control Bus, except during DMA operations when the ISB-3400 has control. The data direction is determined by such signals as Read ($\overline{RD}$), Write ($\overline{WR}$) and Interrupt Acknowledge ($\overline{INTAK}$). The Data Bus uses high-level active logic levels. All cards are required to release the bus to a high impedance state when not in use. The Processor card releases the data bus in response to Bus Request ($\overline{BUSRQ}$) input from an alternate system controller, as in DMA transfers. The ISB-3400 takes control of the data bus during DMA transfers.
A0–A15	15–30	*Address Bus* – A 16-bit tri-state high-level active bus. The address will originate at the processor card or a bus controlling device. The processor card releases the Address Bus in response to a Bus Request ($\overline{BUSRQ}$) input from an alternate controller. The ISB-3400 drives the address bus during DMA transfers. The Address Bus provides 16 address lines for decoding by either memory or I/O. Memory request ($\overline{MEMRQ}$) and I/O request ($\overline{IORQ}$) control lines are used to distinguish between the two operations. The ISB-3400 uses only the lower 8 bits during an I/O Request operation from the CPU (DMA inactive).
$\overline{WR}$	31	*Write to Memory or I/O* – A tri-state, active-low control line that indicates the BUS holds valid data to be written in the addressed memory or output device. The ISB-3400 controls this line during DMA transfers.
$\overline{RD}$	32	*Read from Memory or I/O* – A tri-state, active-low control line that indicates the processor or other bus controlling device wants to read data from memory or an I/O device. The selected I/O device or memory should use this signal to gate data onto the BUS. The ISB-3400 controls this line during DMA transfers.
$\overline{IORQ}$	33	*I/O Address Select* – A tri-state, active-low processor output control line. $\overline{IORQ}$ indicates that the address lines hold a valid I/O address for an I/O Read or Write. The ISB-3400 controls this line during DMA transfers.
$\overline{MEMRQ}$	34	*Memory Address Select* – A tri-state, active-low memory request line. $\overline{MEMRQ}$ indicates that the Address Bus holds a valid address for memory read or memory write operations. The ISB-3400 controls this line during DMA transfers.
$\overline{IOEXP}$	35	*I/O Expansion* – An active-low control signal used to expand or enable I/O Port addressing. $\overline{IOEXP}$ must be low to address the ISB-3400 as an I/O device.
$\overline{MEMEX}$	36	*Memory Expansion* – An active-low control signal used to expand or enable memory addressing. (Not used on the ISB-3400).
$\overline{REFRESH}$	37	*Dynamic Memory Refresh* – A tri-state, active-low control line normally used to refresh dynamic memory. This signal is generated on the processor card. (Not used on the ISB-3400).
$\overline{MCSYNC}$	38	*Machine Cycle Sync* – A tri-state, active-low processor output signal that occurs once during each processor machine cycle. (Machine cycle is defined as the sequence that involves Addressing, Data Transfer and Execution.) $\overline{MCSYNC}$ defines the beginning of the machine cycle. The ISB-3400 uses this line to control wait state generation.
$\overline{STATUS\ 1}$	39	*Status Control Line 1* – Status Control lines provide timing information related to special cycle operations. STATUS 1 is a signal to identify Instruction Fetch. The ISB-3400 uses this line to start interrupt priority identification in a Z80 processor system. In an 8085 processor system this line is used along with STATUS 0 to start interrupt priority identification.

TABLE 3. ISB-3600 STD BUS Signal Definitions (Continued)

SIGNAL	PIN NO.	FUNCTIONAL DESCRIPTION
$\overline{\text{STATUS 0}}$	40	*Status Control Line 0* – In an 8085 processor system, this line is used along with $\overline{\text{STATUS 1}}$ to start interrupt priority identification. It is not used by ISB-3400 is a Z80 processor system.
$\overline{\text{BUSAK}}$	41	*Bus Acknowledge* – An active-low output line from the CPU. The processor responds to a $\overline{\text{BUSRQ}}$ by releasing the bus and giving an Acknowledge signal on the $\overline{\text{BUSAK}}$ line. $\overline{\text{BUSAK}}$ occurs at the completion of the current machine cycle. The ISB-3400 uses this line to activate a DMA transfer if it has requested use of the bus.
$\overline{\text{BUSRQ}}$	42	*Bus Request* – An active-low input line. A $\overline{\text{BUSRQ}}$ causes the processor to suspend operations on the BUS by releasing all tri-state BUS lines for use by another processor. The BUS is released once the current machine cycle is completed. The ISB-3400 asserts this line before executing a DMA transfer.
$\overline{\text{INTAK}}$	43	*Interrupt Acknowledge* – An active-low output line from the processor card that occurs in response to ($\overline{\text{INTRQ}}$). It is used to tell the interrupting device that the processor card is ready to respond to the Interrupt. For vectored interrupts the vector address is placed on the Data Bus by the interrupting device during $\overline{\text{INTAK}}$. The ISB-3400 will output a vector address on the Data Bus if it is the highest priority interrupting card.
$\overline{\text{INTRQ}}$	44	*Interrupt Request* – An active-low processor card input line that conditionally interrupts the program. It is masked and ignored by the processor unless deliberately enabled by a program instruction. If the processor accepts the interrupt, it acknowledges by dropping $\overline{\text{INTAK}}$. The ISB-3400 uses this line to interrupt the processor when certain pre-programmed conditions are met relating to DMA or floppy disk operations.
$\overline{\text{WAITRQ}}$	45	*Wait Request* – An active-low input line to the processor that suspends processor operations as long as it remains low. The processor will hold in a state that maintains a Valid Address on the Address Bus. The ISB-3400 can assert this line from zero to 4 clock cycles in duration.
$\overline{\text{NMIRQ}}$	46	*Non-Maskable Interrupt* – An active-low processor card interrupt input line of highest priority. (Not used on the ISB-3400).
$\overline{\text{SYSRESET}}$	47	*System Reset* – An active-low output from the system reset circuit. The system reset circuit is triggered by power-on detection or by the pushbutton reset. The system reset bus line should be applied to all cards on the BUS that have latch circuits requiring initialization. On the ISB-3400, the floppy disk controller circuit is reset and the external latch is cleared.
$\overline{\text{PBRESET}}$	48	*Push Button Reset* – An active-low input line to the system reset circuit. (Not used on the ISB-3400).
$\overline{\text{CLOCK}}$	49	*Clock From Processor* – A buffered processor clock signal used for system synchronization or as a general clock source. This signal provides timing for the DMA controller on the ISB-3400.
$\overline{\text{CNTRL}}$	50	*Control* – An external clock input for special clock timing. (Not used on the ISB-3400).
PCO	51	*Priority Chain Output (Output, active-high)* – This signal is sent to the PCI input of the next lower card in the priority chain. A card that needs priority should hold PCO low.
PCI	52	*Priority Chain In (Input, active-high)* – This signal is provided directly from the PCO of the next higher card in the priority chain. A high level on PCI gives priority to the card sensing the PCI input.
AUX GND	53 & 54	*Auxiliary Ground* – Ground for AUX Power. Both pins bussed together for current capacity. (Not used on the ISB-3400).
AUX +V	55	*Auxiliary Positive Voltage (+12 Volts DC).* (Not used on the ISB-3400).
AUX –V	56	*Auxiliary Negative Voltage (–12 Volts DC).* (Not used on the ISB-3400).

TABLE 4. ISB-3400 Disk I/O Connector Pin List

PIN NO.	NAME	OPTIONS	PIN NO.	NAME	OPTIONS
2*+	WRITE CUR	ALT I/O (8 INCH)	26	DRIVE SELECT 0	
4+	FAULT RESET	ALT I/O (8 INCH)	28	DRIVE SELECT 1	
6+	ALT I/O	ALT I/O (8 INCH)	30	DRIVE SELECT 2	
8+	ALT I/O	ALT I/O (8 INCH)	32+	DRIVE SELECT 3	MOTOR ON (5.25 INCH)
10	TWO SIDED				
12			34	DIRECTION	
14+	SIDE SELECT		36	STEP	
16			38	WRITE DATA	
18+	HEAD LOAD	ALT I/O (5.25 INCH)	40	WRITE GATE	
20+	INDEX	ALT I/O (5.25 INCH)	42	TRACK 00	
22+	READY	ALT I/O (5.25 INCH)	44	WRITE PROTECT	
24+	INDEX (5.25 INCH)		46	READ DATA	
			48+		ALT I/O (8, 5.25 INCH)
			50+		ALT I/O (8, 5.25 INCH)

*Odd numbered pins are connected to logic ground.

+The logic signals on these pins can be reassigned among each other by means of an on-board jumper area.

TABLE 5. ISB-3400 DC Characteristics

PARAMETER	LIMITS
Power, V_{CC}	5V ±5%
Operating Temperature	0°C to 55°C
Input Loading	
STD BUS	1 LS* Load Max.
Disk Drive	1 LS* Load Max.
Output Drive	
STD BUS	60 LS* Load Max.
Disk Drive	10 TTL Load Min.
Output Tri-State Leakage	1 LS* Load Max.

*Low-power Schottky TTL.

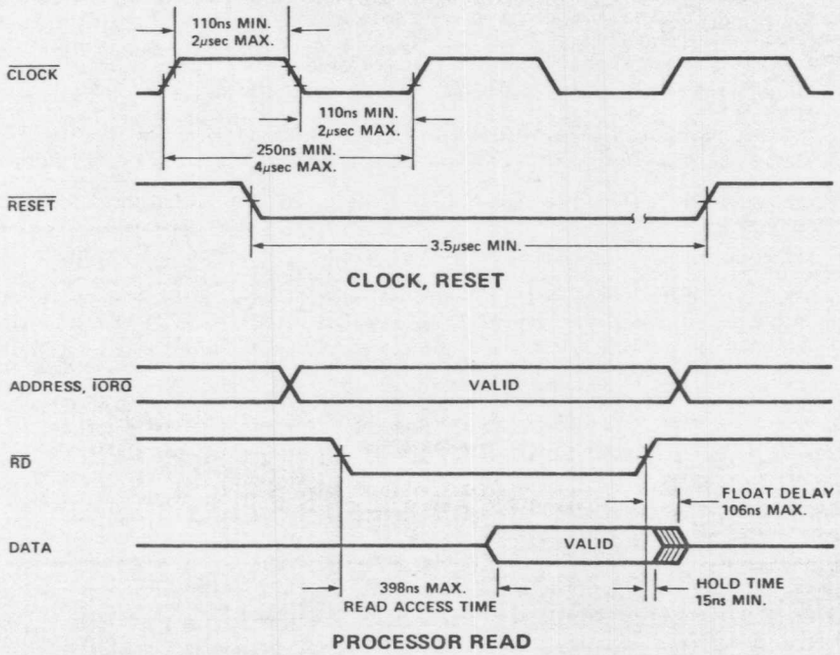
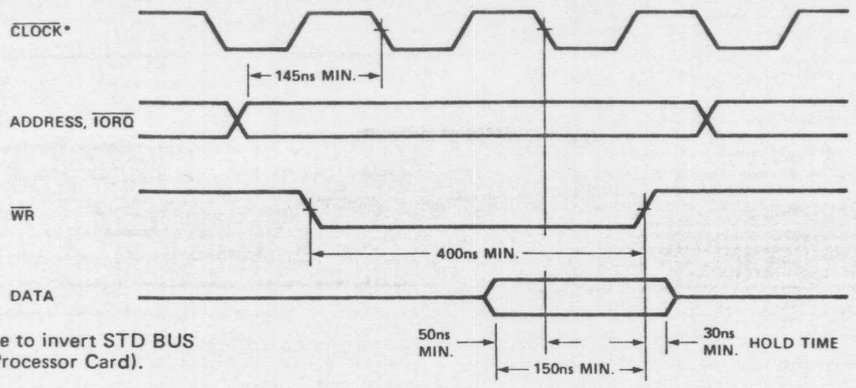
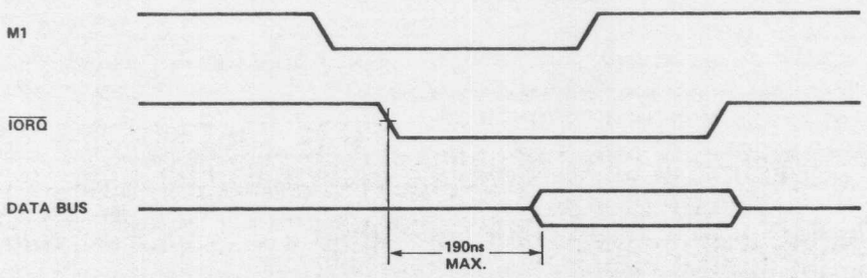


FIGURE 3. ISB-3400 Timing Diagrams

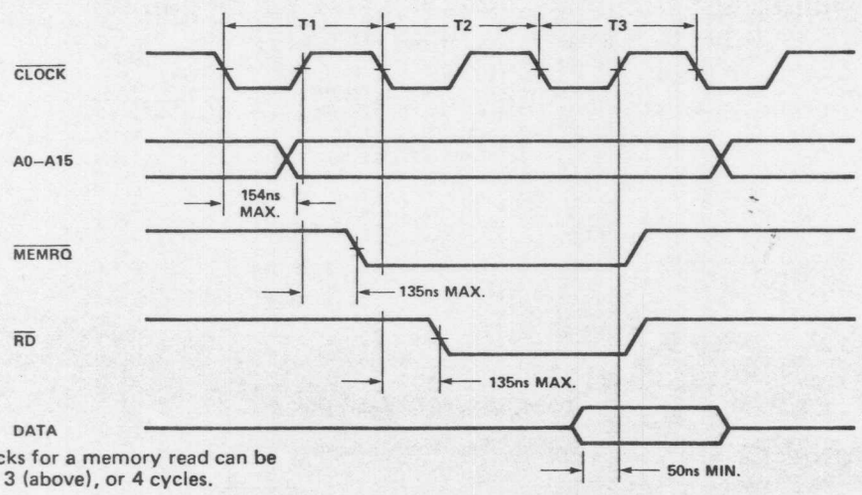


*A jumper option is available to invert STD BUS clock polarity (e.g., 8085 Processor Card).

PROCESSOR WRITE

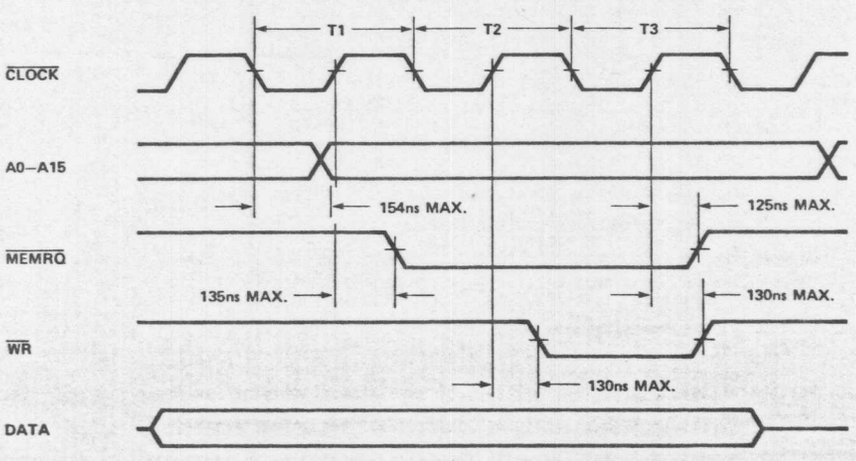


INTERRUPT ACKNOWLEDGE



NOTE: The number of clocks for a memory read can be programmed for 2, 3 (above), or 4 cycles.

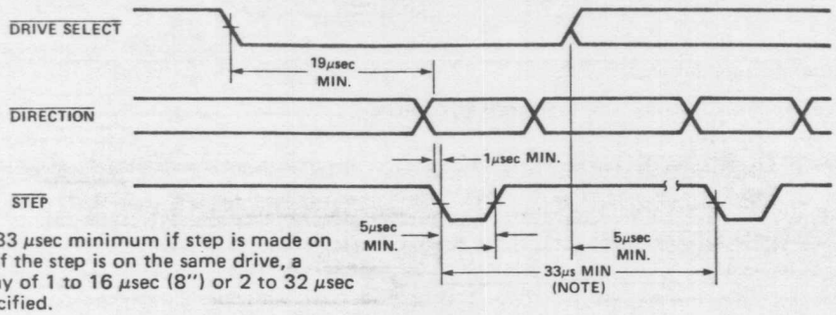
DMA MEMORY READ



NOTE: The number of clocks for a memory write can be programmed for 2, 3 (above), or 4 cycles.

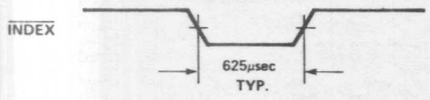
DMA MEMORY WRITE

FIGURE 3. ISB-3400 Timing Diagrams (Continued)

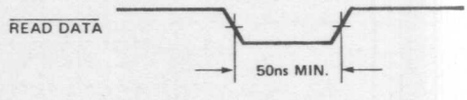


NOTE: Step cycle time is 33 μsec minimum if step is made on a different drive. If the step is on the same drive, a programmable delay of 1 to 16 μsec (8") or 2 to 32 μsec (5.25") can be specified.

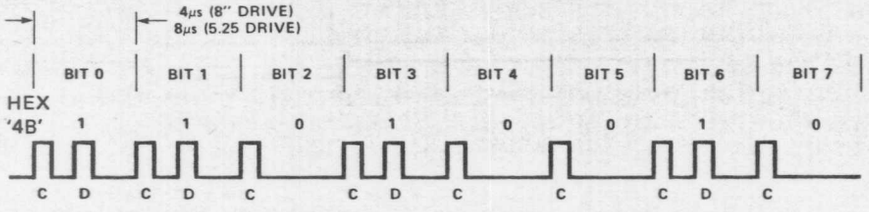
FLOPPY DISK SEEK



FLOPPY DISK INDEX PULSE

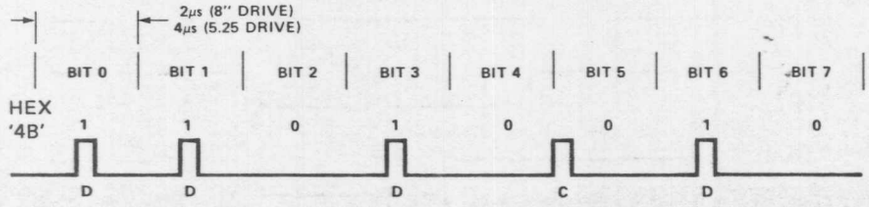


FLOPPY DISK READ DATA



RULE: 1) Write data bits at center of bit cell if a "1"
2) Write clock bits at leading edge of the bit cell

SINGLE DENSITY (FM) DATA FORMAT



RULE: 1) Write data bits at center of bit cell if a "1"
2) Write clock bits at leading edge of bit cell if:
A) No data bit has been written last cell–and–
B) No data bit will be written this cell.

DOUBLE DENSITY (MFM) DATA FORMAT

FIGURE 3. ISB-3400 Timing Diagrams (Continued)

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